Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PADFUNCTIONS:**

1. **1A**
2. **1B**
3. **1CLR**
4. **1N.Q**
5. **2Q**
6. **2CEXT**
7. **2REXT/CEXT**
8. **GND**
9. **2A**
10. **2B**
11. **2CLR**
12. **2N.Q**
13. **1Q**
14. **1CEXT**
15. **1REXT/CEXT**
16. **VCC**

**.067”**

**6**

**7**

**8**

**9**

**1**

**16**

**15**

**14**

**2 3 4 5**

**13 12 11 10**

**DIE ID**

**123**

**LS**

**.059”**

**Top Material: Al**

**Backside Material: Si Ni**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: LS 123**

**APPROVED BY: DK DIE SIZE .059” X .067” DATE: 7/18/18**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: 54LS123**

**DG 10.1.2**

#### Rev B, 7/19/02